Arguments/Remarks

The rejection of independent claims 7 and 14, and dependent claims 8, 10, 11, 12, 15, 16, 18, 19, and 20 under 35 U.S.C. § 102(a) as being anticipated by Marinko et al. (US 6,566,239) is respectfully traversed. As an initial matter, it should be observed that Applicant's invention provides a fabrication method of a semiconductor package substrate having contact pad protective layer formed thereon. More specifically, the conductive film served as entire connection is formed in the process for fabricating the patterned circuit and conductive vias, and the second resist layer is additionally formed to cover other conductive trace areas outside the contact pads. Alternatively, the contact pads may be formed only on the substrate. Then, a metal barrier layer is formed on the contact pads, while the conductive trace, the conductive vias, the contact pads as well as the metal barrier layer thereon are formed in the substrate.

Marinko et al. discloses a method of forming a redistribution layers (wirings) and a sealing resin at the wafer level, comprising the following steps:

> An insulating film (el. 13) has an opening formed at a position corresponding to an electrode pad (el. 12). Then, a metal film (el. 14), made of copper, is formed all over the wafer (el. 11) and beneath a wiring film (el. 17) in order to form a wiring (el. 25). A resist (el. 15), made of an insulating material is provided on the underlying metal film (el. 14), and has an opening (el. 16) shaped according to the wiring (el. 25) to be formed. Using the resist (el. 15) as a mask and the metal film (el. 14) as an electrode, a wiring film (el. 17) is formed by an electroplating process. The resist (el. 15) is removed once the wiring film (el. 17) is formed. A resist (el. 18), provided on the underlying metal film (el. 14) and the wiring film (el. 17,) has an opening (el. 19) to form a post (el. 20) therein. Subsequently, a Ni film (el. 21) and an Au film (el. 22) are formed on the post (el. 20) in proper order to form a post terminal (el. 23). After the wiring (el. 25) is formed on the post (el. 20), the sealing resin (el. 26) is formed over the wafer (el. 11).

Despite the fact that wafer level technique employed in Makino et al. should not apply to chip-level package sufficiently, there are several things that seems to be misunderstand by the Examiner. For instance, several elements disclosed in Makino et al. are modified/changed to a physically or functionally familiar element in the Office Action. By reviewing the following corresponding text (FIG 3A-3l) from the present invention with the steps cited from the Office Action (page 2 and 3) and the associated text of cited reference (Makino et al.), the difference can be shown distinctly as follows.

In the present invention, an insulating layer (el. 30), which may be formed with multiple trace layers on the substrate, is provided with a plurality of insulating vias (el. 301) formed therein to expose an inner trace (el. 30a) underneath the insulating layer; the conductive film (el. 31) provides a current conductive path, including the patterned trace layer and the barrier layer, for subsequent electroplating of metal layers; the conductive layer (el. 31) may be made of metal alloy and a stack of several metal layers; the first resist layer (32), covering the conductive film (el. 31), has a plurality of openings (el. 320) formed by patterning process; conductive vias (el. 302) are formed in the opening (el. 320) and insulating vias (el. 301) by the electroplating process; the patterned trace layer (el. 33) has a plurality of contact pads (el. 330) formed in the conductive vias (el. 302) to establish connection with the inner trace (el. 30a); the contact pad (el. 330) may also be connected to the inner trace (el. 30a) via lead traces of the patterned trace layer (el. 33); the second resist layer (el. 34) is formed to cover the patterned trace layer (el. 33) outside the contact pad (el. 330); a plurality of openings (el. 320) formed by patterning process in the second resist layer (el. 34); a metal barrier layer (el. 35) covers thoroughly the surface of the contact pad (el. 330); therefore the current conduction path includes the conductive film (el. 31), the conductive vias (el. 302), and the contact pads (el, 330); then, the second resist layer and the first resist layer are then removed; eventually, a solder mask (el. 36) is coated on the package substrate to protect the package substrate from external environment contamination; in addition, a plurality of opening (el. 3600) may be formed in the solder mask (el. 36) to expose the contact pads (el. 320). Thereby, these characteristics steps of the present invention should be distinguishable from the disclosure of Makino et al., doubtlessly.

Further, it is noted that the following sentences quoted from the Office Action (page 2; line 2-5), "... to form a patterned trace layer (el. 17) in the opening and in the blind vias to form conductive vias, wherein the patterned trace layer comprises a plurality of contact pads,

and at least one of the contact pads is electrically connected to at least one of the conductive vias" are not found in Makino et al. instead; these are found in the present invention on page 11, lines 18-24 of the specification which recites " ...to form the patterned trace layer (el. 33) and the conductive vias (el. 302) in the opening (el. 320) and insulating vias (el. 301), respectively. The patterned trace layer (el. 33) has a plurality of contact pads (el. 330) formed in the conductive vias (el. 302) to establish connection with the inner trace (el. 30a). The conductive vias (el. 302) may be formed directly below the contact pad (el. 330). The contact pad (el. 330) may also be connected to the inner trace (e1. 30a) via lead traces of the patterned trace layer (el. 33)".

Similarly, a peccadillo/ vague meaning is also found in the following sentences, quoted from the Office Action (page 3; line 9), "removing the second resist layer (Fig. 8-9), the first resist layer (Figs. 3-4)...". As stated in Makino et al, the first resist layer (el. 15) is removed right after the formation of the wiring (el. 25). Accordingly, in forming metal members, a resist has to be provided and then removed each time, which results in complicating the process of manufacturing a semiconductor device. In contrast, the present invention provides an improved and useful method to simplify such process.

Furthermore, it should be point out that the Examiner misapprehends the electrode pad (e1.12 of Makino et al.) as the contact pad (el. 330 of the present invention). The component corresponding to that electrode pad (e1.12 of Makino et al.) is actually the inner trace (el. 32a) of the present invention. Thus, said contact pad (el. 330) is a characteristic part of the present invention. Moreover, the applicant also disagrees with the Examiner's allegation that the resist (el. 18 of Makino et al) is equivalent to the second resist layer (el. 34 of the present invention). Since the first resist layer (el. 15 of the present invention) is not removed at that time the resist (el. 18 of Makino et al) is removed, a distinctive structure is formed thereafter. As a result, the present invention is not anticipated by the disclosure of Makino et al.

The rejections of claims 9 and 17 under 35 U.S.C. § 103(a) as unpatentable over Makino in view of Shinomiya (5,907,786), and of claim 13 under 35 U.S.C. § 103(a) as unpatentable over Makino in view of Wang et al. (2004/0000427) are both respectfully traversed.

Ipso facto, even if Makino et al. is combined with either Shinomiya or Wang et al, the combination still fails to teach or suggest a inventive and useful fabrication method of a semiconductor package substrate having contact pad protective layer formed thereon. Furthermore, one skilled in the art might lack motivation or disable to deduct those characteristic inventive steps of the present invention from these reference documents, such as forming the multiple layers of thin trace structures on the substrate; forming the conductive vias in the insulating layer, and forming a metal barrier layer, with a similar dimension as the contact pad, on the contact pad of the patterned trace structure. Furthermore, the present invention discloses a new electroplating method to ameliorate the problems such as reducing the effective wiring area for the package substrate and the signal interference, while the reference documents do not.

Applicants believe the application is in condition for allowance and respectfully solicit a Notice of Allowance.

The Commissioner is hereby authorized to charge any fee which should have been filed herewith to our Deposit Account No. 50-0337, under Order No. 7452-105/10313554. A duplicate copy of this paper is enclosed.

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Respectfully submitted,

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